WHAT IS CLAIMED IS:

1. A current compensation circuit for use with a current mirror circuit, the current mirror circuit having a current path defined by a first current mirror stage driving a second current mirror stage, the second current mirror stage coupled to a supply voltage source, the current compensation circuit comprising:

an impedance divider coupled to the supply voltage and having an output node, the impedance divider operative to generate a compensation signal at the node representative of voltage changes in the supply voltage source; and

a gain stage having an input coupled to the output node and a current output connected to the current path, the gain stage operative to generate a compensation current for application to the current path in response to the compensation signal.

2. A current compensation circuit according to claim 1 wherein the gain stage comprises:

a common-source gain stage.

3. A current compensation circuit according to claim 2 wherein the common source gain stage comprises:

a first parallel array of programmable transistors for defining a predetermined range of compensation current.

4. A current compensation circuit according to claim 3 wherein the common source gain stage further comprises:

a second parallel array of programmable transistors to cooperate with the first parallel array of transistors for defining a predetermined gain characteristic for the compensation current.

5. A current compensation circuit according to claim 1 wherein the impedance divider comprises:

at least two impedance elements coupled in series between the supply voltage source and a return voltage source

6. A current compensation circuit according to claim 1 wherein the current compensation circuit is formed on a single integrated circuit device.

7. A current compensation circuit according to claim 6 wherein the current compensation circuit is formed in CMOS.

8. A current compensation circuit according to claim 7 wherein the first array of transistors are p-channel transistors, and the second array of transistors are n-channel transistors.

9. A current compensation circuit for use with a current mirror circuit, the current mirror circuit having a current path defined by a first current mirror stage driving a second current mirror stage, the second current mirror stage having a source connection tied to a supply voltage source, the current compensation circuit comprising:

means for detecting changes in the supply voltage from the supply voltage source, the means for detecting changes including means for generating a compensation signal representative of voltage changes in the supply voltage source; and

means for generating a compensation current for application to the current mirror in response to the compensation signal.

10. A current compensation circuit according to claim 9 wherein the means for detecting changes in the supply voltage comprises:

an impedance divider coupled to the supply voltage and having an output node, the impedance divider operative to generate a compensation signal at the node representative of voltage changes in the supply voltage source.

11. A current compensation circuit according to claim 9 wherein the means for generating a compensation current comprises:

a common source gain stage having an input coupled to the output node and a current output connected to the current mirror, the common source gain stage operative to generate a compensation current for application to the current mirror current path in response to the compensation signal.

12. A current compensation circuit according to claim 9 and further including:

means for setting the range of available compensation current from the current source.

13. A current compensation circuit according to claim 9 and further including:

means for setting the gain of the common source gain stage.

14. A method for compensating for supply-voltage-induced changes to current from a current mirror, the method including the steps:

detecting changes in the supply voltage from a supply voltage source;

generating a compensation signal representative of the voltage changes in the supply voltage source; and

generating a compensation current for application to the current mirror in response to the compensation signal.

15. A timing generator for use in a semiconductor tester, the timing generator including:

a delay line having a plurality of delay cells with respective phase-shifted outputs and bias current inputs;

a selector having a plurality of inputs for receiving the phase shifted outputs, and an output;

phase detection circuitry for detecting the phase shift between the selector output and a reference signal, and generating bias current; and

fanout circuitry to distribute the bias current to the plurality of delay cells, the fanout circuitry comprising a first current mirror circuit and a second current mirror circuit coupled to a supply voltage, the current mirror circuits cooperating to define a bias current path, and

a current compensation circuit coupled to the fanout circuitry to minimize changes to the bias current resulting from changes in the supply voltage.

16. A timing generator according to claim 15 wherein the current compensation circuit comprises:

an impedance divider coupled to the supply voltage and having an output node, the impedance divider operative to generate a compensation signal at the node representative of voltage changes in the supply voltage source; and

a gain stage having an input coupled to the output node and a current output connected to the current path, the gain stage operative to generate a compensation current for application to the current path in response to the compensation signal.

17. A timing generator for use in a semiconductor tester, the timing generator including:

a delay line having a plurality of delay cells with respective phase-shifted outputs and bias current inputs;

a selector having a plurality of inputs for receiving the phase shifted outputs, and an output;

phase detection circuitry for detecting the phase shift between the selector output and a reference signal, and generating bias current; and

means for distributing the bias current to the plurality of delay cells.

18. A timing generator according to claim 17 wherein the means for distributing comprises:

fanout circuitry to distribute the bias current to the plurality of delay cells, the fanout circuitry comprising

a first current mirror circuit,

a second current mirror circuit coupled to a supply voltage, the first and second current mirror circuits cooperating to define a bias current path, and

a current compensation circuit comprising

an impedance divider coupled to the supply voltage and having an output node, the impedance divider operative to generate a compensation signal at the node representative of voltage changes in the supply voltage source; and

a common source gain stage having an input coupled to the output node and a current output connected to the current mirror, the common source gain stage operative to generate a compensation current for application to the current mirror current path in response to the compensation signal.

19. A timing generator according to claim 18 wherein the gain stage comprises:

a common-source gain stage.